CONTENTS

[1] Scope of Application

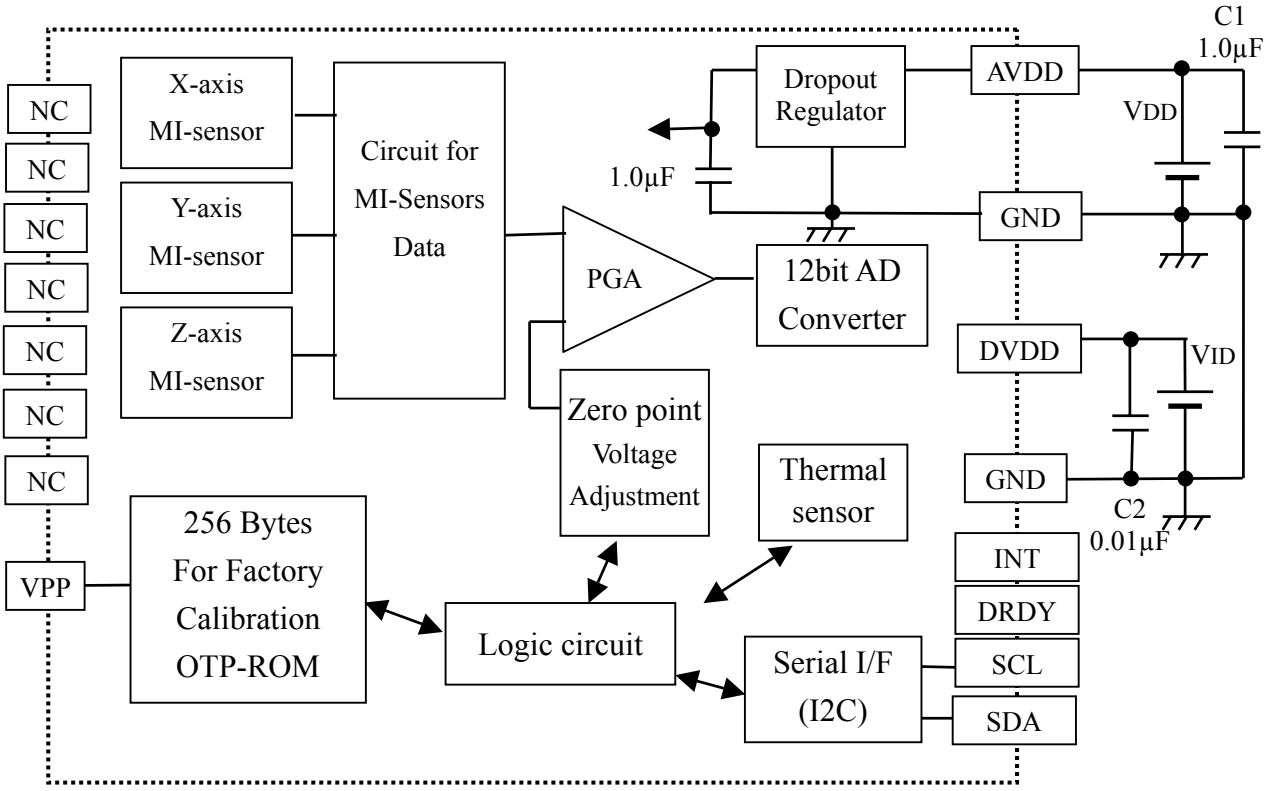
This specification applies to the 3-axis magnetic sensor AMI305 provided to ＊＊＊ by Aichi Steel Corporation.

[2] General Description

The AMI305 is an intelligent electronic compass that integrates three Magneto-Impedance sensor elements (MI-element) with their controller IC in a single small package.

The controller IC of the AMI305 consists of a circuit for detecting the magnetic signals from three MI-sensor elements, an amplifier capable of compensating each sensors offset and setting appropriate sensitivity values, a thermal sensor for measuring the ambient temperature, a 12bit AD converter, an I2C serial interface circuit and a constant voltage circuit for power control.

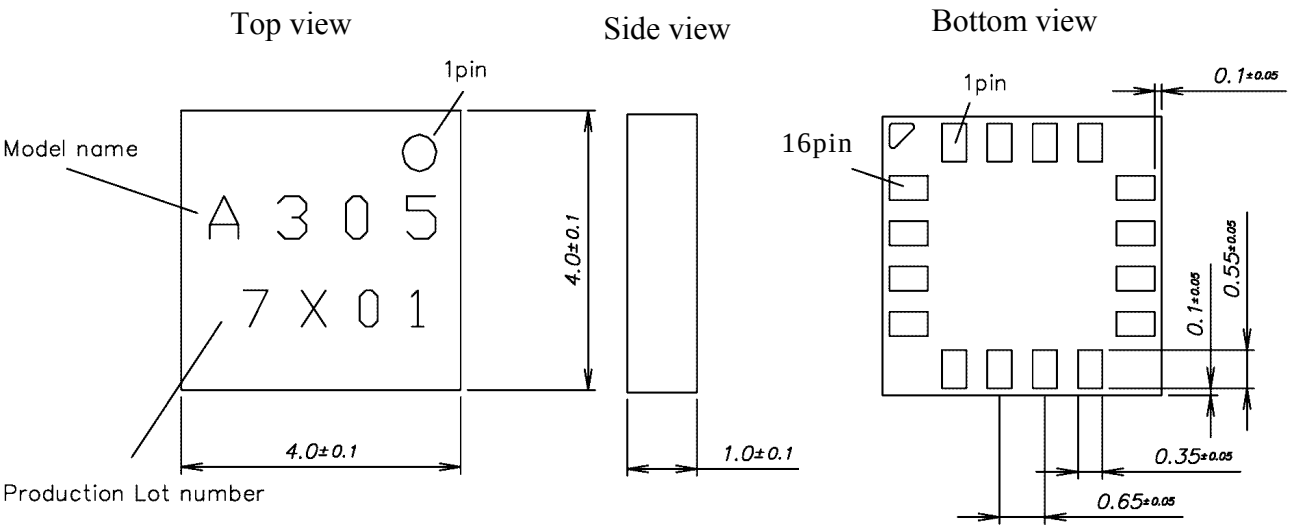
[3] Block Diagram



Note)

The control signals SCL and SDA, are not tolerant of voltages more than DVDD + 0.3 volts. If DVDD is removed, the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes.

[4] Dimensions and marking Layout



[5] Pin Description

Name	Pin No.	I/O	Description	Reference
DVDD	1	Power	Digital Circuit Power Input	Please mount a 0.01μF bypass capacitor between DVDD and DGND.
GND	2	Power	Digital Circuit Power Ground	
AVDD	3	Power	Analog Circuit Power Input	Please mount a 1.0μF bypass capacitor between AVDD and AGND.
GND	4	Power	Analog Circuit Ground Input	
NC	5-11	-	Non-Connection	—
Vpp	12	-	Testing Pin	Use as Non-Connection (NC).
INT	13	Output	Interrupt Pin	—
DRDY	14	Output	Completion of Measurement	—
SCL	15	Input & Output	I2C Signal Clock I/O	—
SDA	16	Input & Output	I2C Signal Data I/O	—

[6] Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to +5.0	V
	V_{ID}	-0.3 to +4.0	V
Storage Temperature	T_{STG}	-40 to + 125	°C
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V

[7] Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.70	2.50	3.60	V
	V_{ID}	1.70	1.80	V_{DD}	V
Operating Temperature	T_{OPR}	-20	—	+85	°C

[8] Electrical Characteristics

(AVDD= +2.50V 、 DVDD= +1.80V 、 1.0μF ceramic capacitor between AVDD－GND)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Average Operating Current at Measurement	I_{DD1}	Output Data Rate = 20SPS, Normal-Mode	—	0.15	1	mA
	I_{ID1}		—	0.1	2.0	μA
Stand-by-mode Operating Current	I_{DD2}	AVDD= +1.7V to 2.9V	—	7	10	μA
	I_{ID2}	—	—	0.1	2.0	μA
OFF-mode Leak Current	I_{DD3}	—	—	—	1	μA
	I_{ID3}	—	—	—	1	μA
ADC Resolution	—	—	12			bit
I2C Operating Frequency	f_{SCL}	—	0	—	400	kHz
Start Condition Set-Time	t_{sta}	—	0.6	—	—	μs
High Level Input Voltage	V_{IH}	—	70% DVDD	—	—	V
Low Level Input Voltage	V_{IL}	—	—	—	30% DVDD	V
High Level Output Voltage	V_{OH}	—	80% DVDD	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = +3mA	—	—	20% DVDD	V
I2C Address	—	—	1Fh/read 1Eh/write			
Turn on time 1	tON1	from Off -mode to Stand-by	—	200	250	μs
Turn on time 2	tON2	from Stand-by –mode to Active–mode	—	—	8	μs
Turn off time 1	tOFF1	from Active -mode to Stand-by –mode	—	—	30	μs

[9] Magnetic Characteristics

(AVDD= +2.50V 、 DVDD= +1.80V 、 1.0μF ceramic capacitor between AVDD－GND)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Moving Range (*1)	Rm	Ta= +25 °C	—	±6.0	—	gauss
Measurable Range (*2)	Ra	Adjust the offset with XOFFSET, YOFFSET, ZOFFSET to prevent from the saturation of output	—	±12	—	gauss
Linearity	Lin	Rm=±3.0gauss、Ta= +25 °C	—	0.5	2	%FS
Output OffsetColtage at Zero Gauss	Vofs	Ta= +25 °C	—	0	—	LSB
		Temperature Drift （Ta= +25 °C Standard Ta=0～+60℃）	-3	—	+3	milligauss /℃
Magnetic Sensitivity	deltaV	Ta= +25 °C	—	300	—	LSB/gauss
		Temperature Drift （Ta= +25 °C Standard、 Ta=0～+60℃）	-7	—	+5	%
Resolution	—	Ta= +25 °C , Rm= ± 0.3gauss at Horizontal plane	—	±0.9	—	degree
Accuracy (*3) (*4)	—	Ta= +25 °C , Rm= ± 0.3gauss at Horizontal plane	—	±0.6	±1.0	degree
ADC throughput	Fr	Ta= +25 °C	—	—	1000	SPS
Maximum Exposed Field	—	No perming effect on zero reading	—	—	10000	gauss

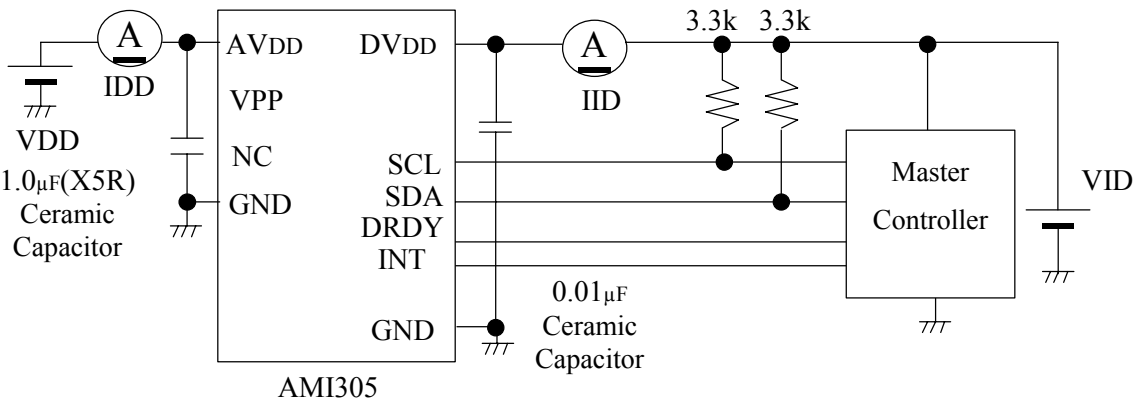
*1: Moving range: preset operating range

*2: Measurable range: overall measurable range within which preset operating range can be fit in by adjusting appropriate offsets.

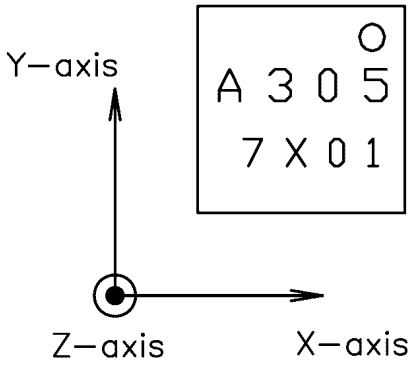
*3: After executing an initial calibration after AMI305 is mounted by the customer

*4: The Cross axial interference correction is done by using "Axis interference" Registers.

[10] Measuring Circuit



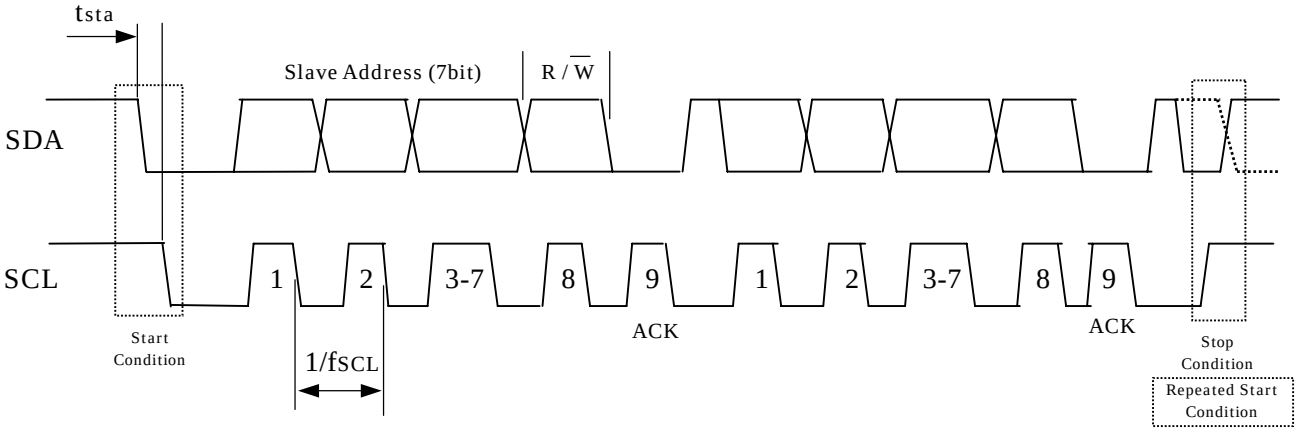
[11] Polarity



When the arrow is directing North output becomes “+”.

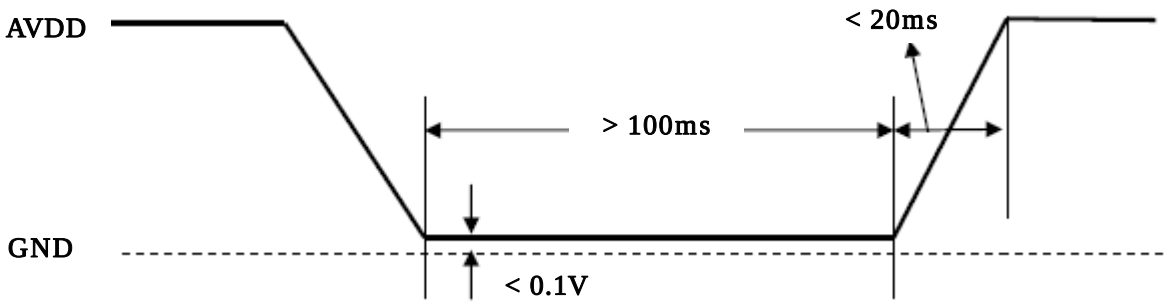
[12] Timing Chart

12-1. I2C Bus Timing Chart



12-2. Power OFF and Power ON

In order to secure stable starting, you have to carry out Power-OFF and Power-ON in the following procedure.



[13] Measurement Timing Diagram

There are two kinds of measurement modes of the following.

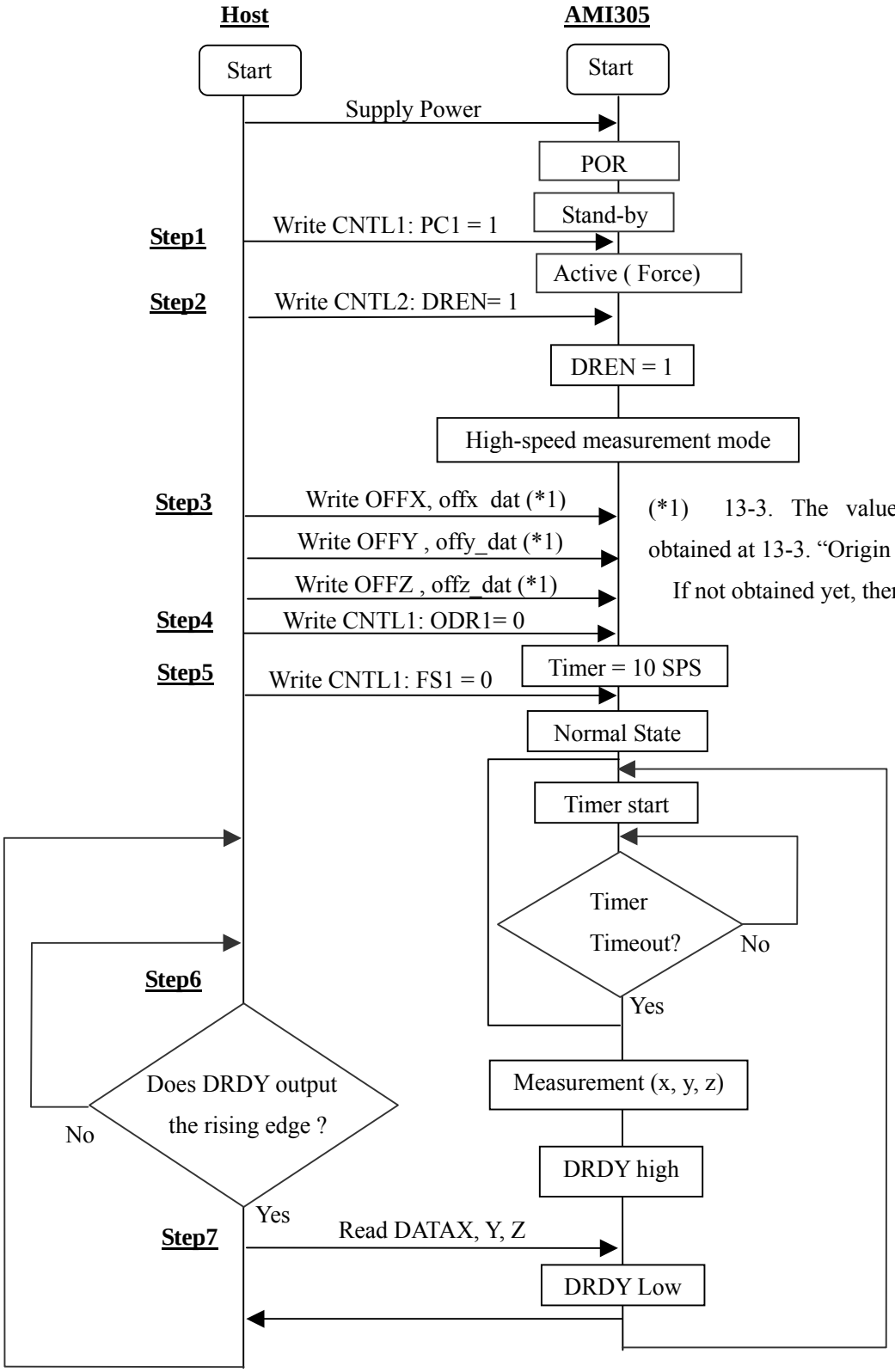
Normal State	AMI305 is measured at specified cycle (10SPS or 20SPS) at the cycle.
Force State	AMI305 is measured by the measurement request from the host.

13-1. Normal State

Normal State sequence

Step1	AMI305 Active (Force State)
Step2	Set DRDY ready function enable
Step3	Set offx_dat, offy_dat, offz_dat
Step4	Set Output Data rate
Step5	Set Normal state
Step6	Does DRDY output the rising edge ?
Step7	Read DATAX, DATAY, DATAZ

13-1. Normal State

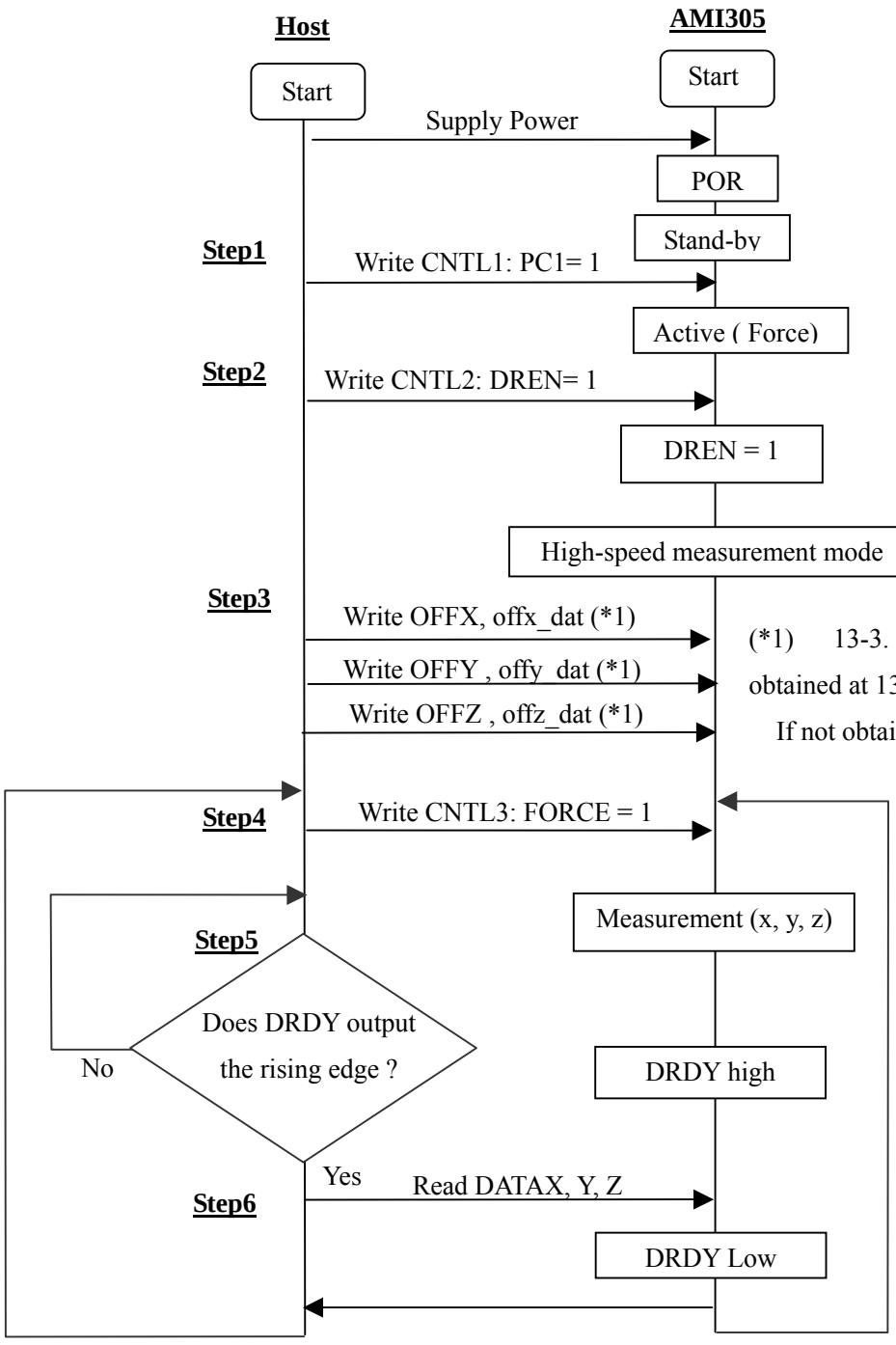


(*1) 13-3. The value is the one obtained at 13-3. “Origin Adjustment” If not obtained yet, then skip.

13-2. Force State

Force State sequence

Step1	AMI305 Active (Force State)
Step2	Set DRDY ready function enable
Step3	Set offx_dat, offy_dat, offz_dat
Step4	Measurement Request
Step5	Does DRDY output the rising edge ?
Step6	Read DATAX, DATAY, DATAZ
Step7	Next Step6



(*1) 13-3. The value is the one obtained at 13-3. “Origin Adjustment” If not obtained yet, then skip.

13-3. Offset Adjusting

13-3-1. Outline of Offset Adjusting

Offset Adjusting is to make the output value around zero under magnetic environment after the implementation by changing movement point electrically.

13-3-2. HOST Parameter

After measuring the following parameter according to the 13-3-3 procedures, HOST should save it in memory, and it is necessary to set after power supply injection of AMI305.

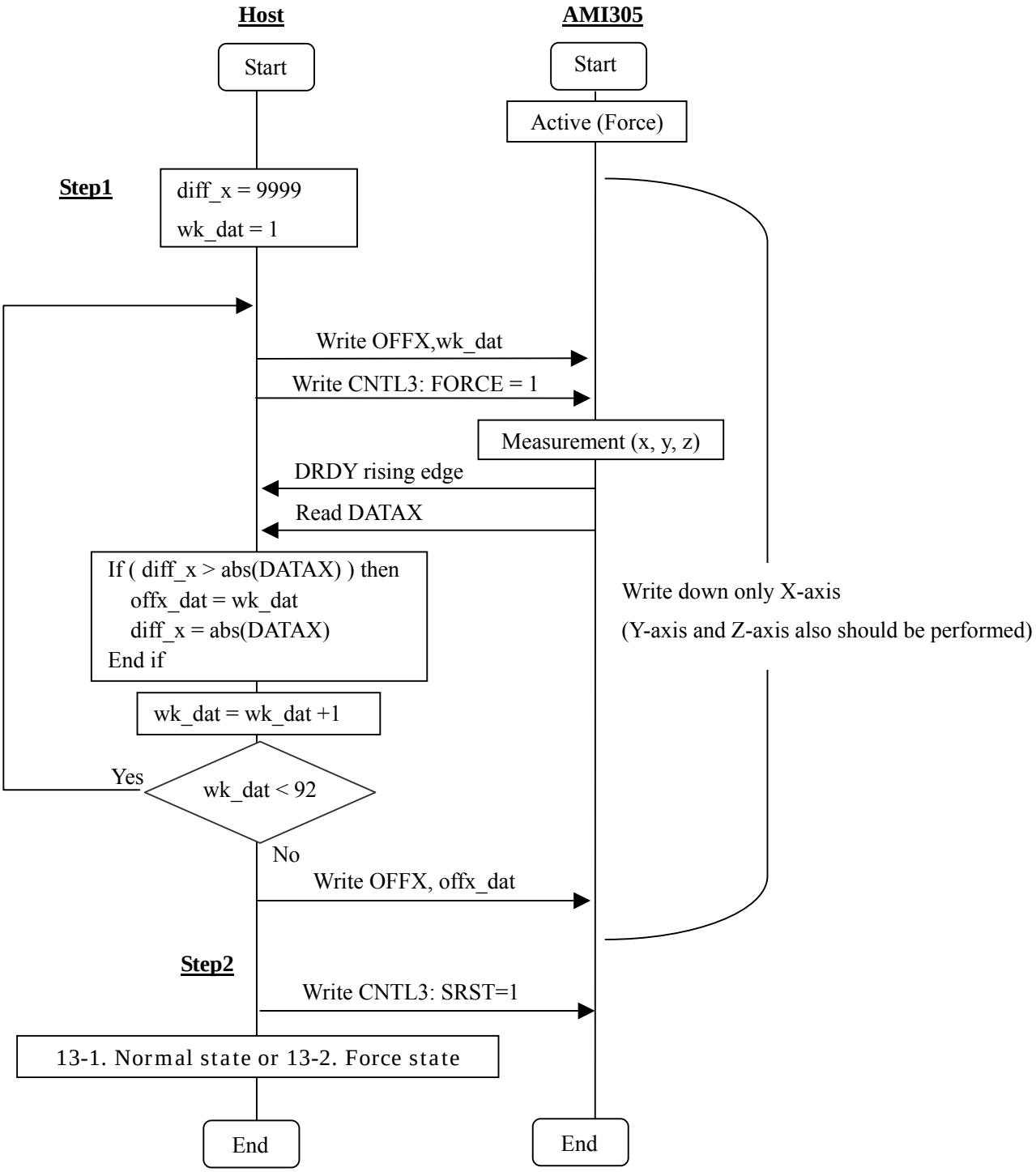
No	Parameter	Contents
1	offx_dat	Adjusted value of X axis offset
2	offy_dat	Adjusted value of Y axis offset
3	offz_dat	Adjusted value of Z axis offset

13-3-3. Procedure

Procedure of Offset Adjusting is as follows.

Step1	offx_dat is obtained by finding the combination of each OFFX:FINE
Step2	Make a soft reset. To 13-1. Normal state or 11-2. Force state

13-3-3. Procedure



13-3-4. Offset registers

There are coarse and fine in the Offset register. Fine is used for the fine-tuning and Coarse is used for the rough tuning.

The table below shows the structure of the Offset X register

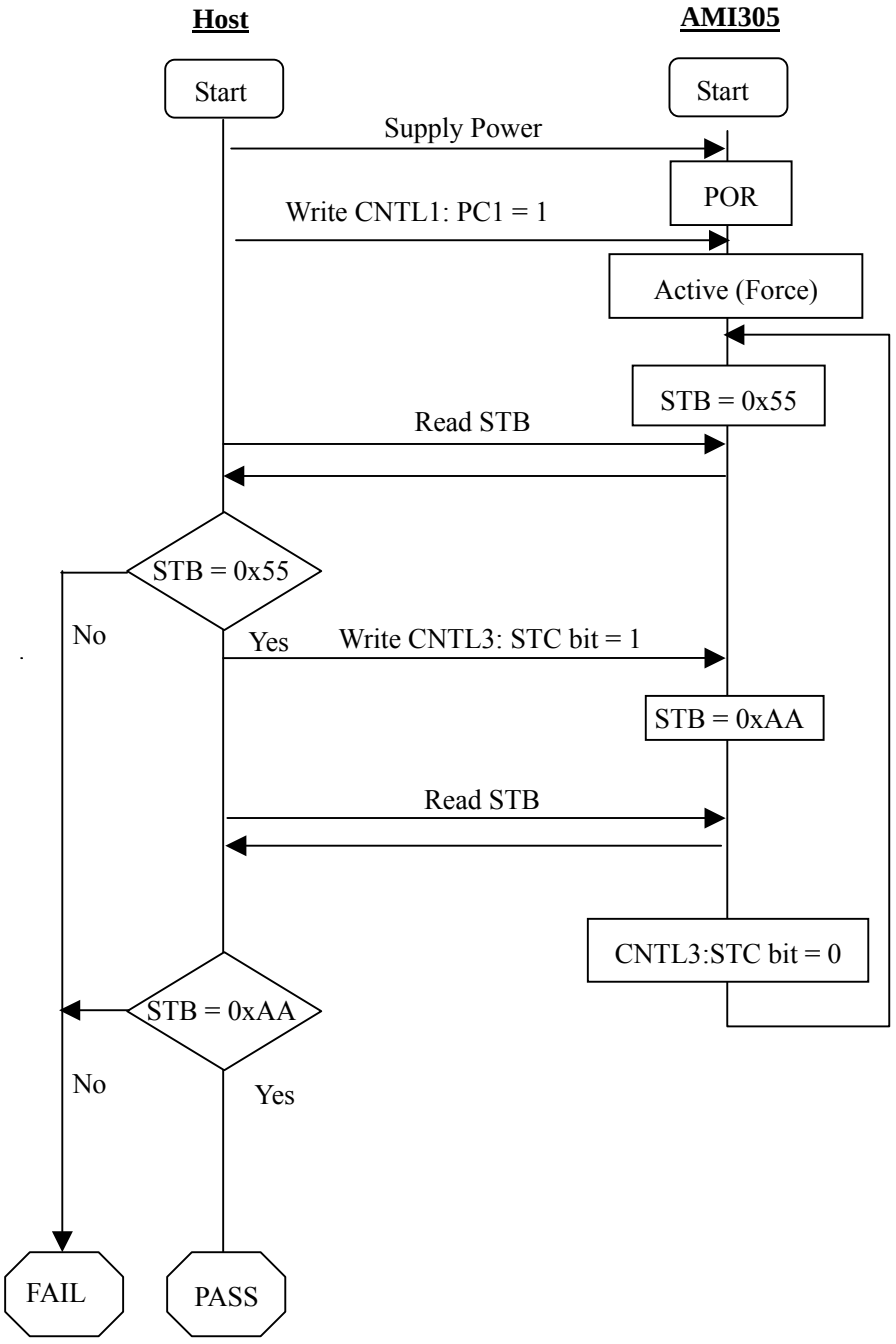
	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
OFFX	0x6C	Reserved	fine						
			X	X	X	X	X	X	X
	0x6D	Reserved							

Offset Y register and Offset Z register have same structure

13-4. Self –test

Self-test capability is used to ensure sensor functionality on test setups; service, production and engine system check purposes. In component level, self-test return simple response from self test response register, this response is compared to known response.

Self –test sequence



[14] Control Interface

14-1. Power Supplies

14-1-1. AVDD

AVDD is main power supply. The AMI305 works by using this power supply current.

14-1-2. DVDD

DVDD gives the voltage reference for digital logic interface.

14-1-3. Internal dropout regulator

AMI305 is equipped with a constant voltage regulator in order to stabilize AVDD power supply.

14-2. I2C slave interface

I2C interface is shown below

Terminal	Content
SCL	I2C Clock
SDA	I2C Data

Master/ slave	Slave only
Address	Consists of 7-bit address. The address of the IC is 0001111b (0x1F/read, 0x1E/write)
Tranfer Rate	Fast mode 400kHz

14-3. Interrupt signal

The interrupt signal monitors the incoming signal level from MI-sensor to the IC. It is the common feature for all measurement modes. If an incoming signal exceeds the preset level, the sequences shown below will be carried out:

(1) Write the INS1 bit of the relevant axis to 1.

(2) Collecting INS1 of each axis and write STA1:INT as OR signal of 3-axis.

(3) Output of STA1:INT(='high') by INT terminal.

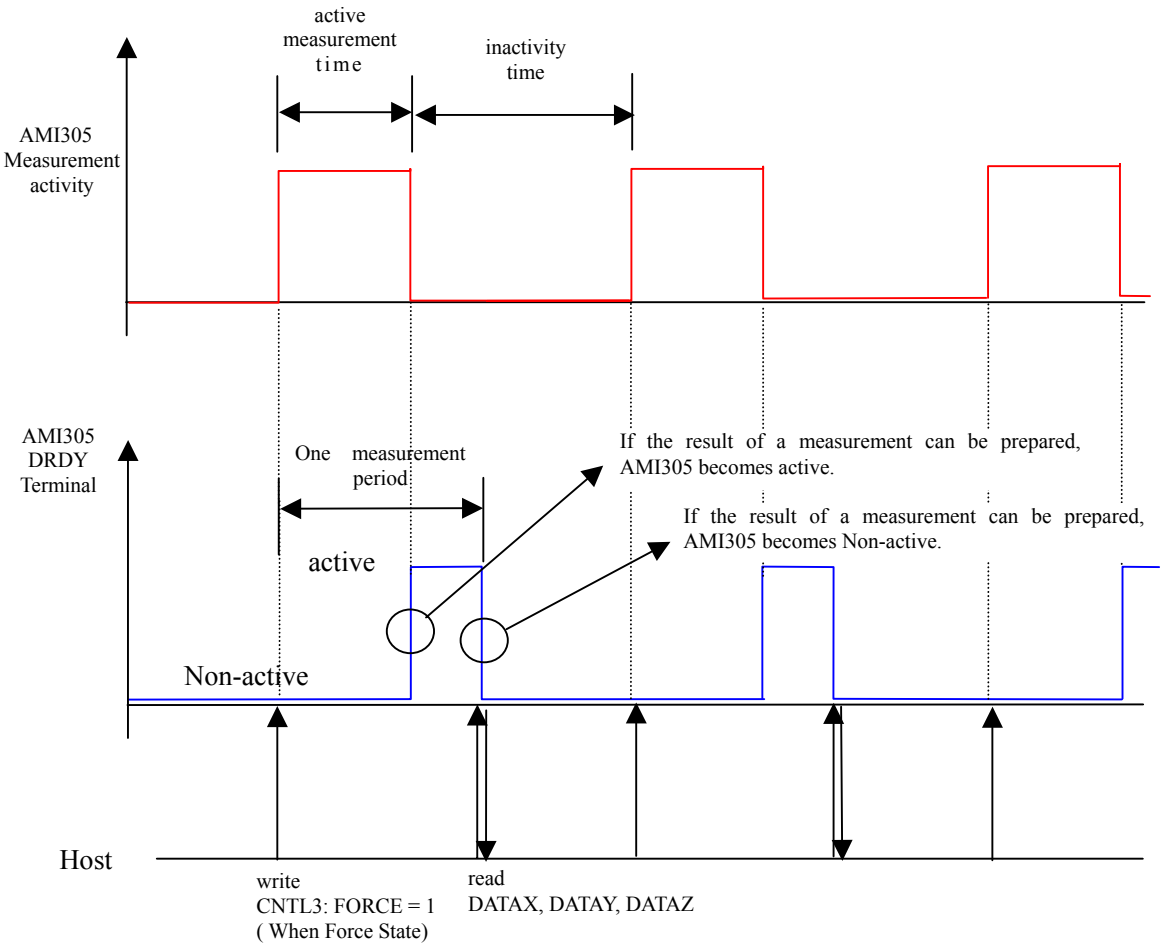
Cancel release is done by reading INL; herewith INS1 of each axis and STA1:INT (INT terminal) are cleared. INS1 tells in which axis the event occurred.

The related registers are as follows:

Register	Register Set Contents
THR1	Preset Level
STA1:INT	Interrupt Occurrence
INS1:PXSI,PYSI,PZSI NXSI,NYSI,NZSI	Interrupt Occurrence of each axis
INL	Interrupt Clear
CNTL2 : IEN	interrupt function Enable/ disable
INC1: XIEN	X interrupt Enable/ disable
INC1: YIEN	Y interrupt Enable/ disable
INC1: ZEN	Z interrupt Enable/ disable
INC1: IEA	INT Terminal Active level Low / High
INC1: IEL	signal latched/one pluse

14-4. DRDY signal

The sequence of DRDY signal is shown below. This signal becomes active after measurement results become available. It turns non-active again with the execution of next measurement.



※In case the measurement results have not been read out during inactivity time, STAT1:DOR is set.

The related registers are as follows:

Register	Content
CNTL2:DREN	DRDY Terminal Enable/ disable
CNTL2:DRP	DRDY Terminal Active Level Low / High
STA1:DRDY	DRDY Status of Terminal
STA1:DOR	Output Data Overrun

14-5. Register

14-5-1. Output register

Output the magnetic measurement results and status.

Magnetic measurement results

DATAX	X channel meas. result
DATAY	Y channel meas. result
DATAZ	Z channel meas. result

Status register(s)

STAT1	Status

14-5-2. Control register

The registers for controlling the IC are as follows

Control register(s)

Power modes	CNTL1
Functional state	CNTL2
Interrupt controls	INC1 / ITHR1

Measure register(s)

Measurement mode	CNTL1/ CNTL3
Preset time	PRET
Temperature	TEMP

[15] Command

15-1. Command Sequence

There are 2 patterns of commands: read command and write command.
Read command is used for reading registers and accessing output values.
Write command is used for register setup.

The command sequences are shown below

15-1-1. Read Command

Master	S	SAD+ W (*1)		RAD		S r	SAD+ R (*1)			A		A		N	P
Slave			A		A			A	RDA1		RDA2		•		

S	Start Condition	SAD + W	slave address + write (0x1E)
Sr	Restart Condition	SAD + R	slave address + read (0x1F)
A	ACK（SDA_Low）	RAD	Read-in address (register)
N	NACK（SDA_High）	RDA1	Read-in data1
N	NACK（SDA_High）	RDA2	Read-in data2
P	Stop Condition		

(*1)

7	6	5	4	3	2	1	0
SAD							W/R

15-1-2. Write Command

Master	S	SAD+W (*1)		WAD		WDA1		WDA2		• • •		P
Slave			A		A		A		A		A	

S	Start Condition	SAD + W	slave address + write (0x1E)
A	ACK（SDA_Low）	WAD	Write-in address (register)
N	NACK（SDA_High）	WDA1	Write-in data 1
N	NACK（SDA_High）	WDA2	Write-in data 2
P	Stop Condition		

(*1)

7	6	5	4	3	2	1	0
SAD							W/R

[16] Register

16-1. Register type

The register types are as follows:

TYPE1	Control and Condition	Unsigned 1 byte (unsigned char).
TYPE2	Temperature	2´s complement signed 1 byte. -128d = 0x80 0d = 0 127d = 0x7F
TYPE3	Output of Magnetism	2´s complement signed 2 byte. -2048d = 0xF800 0d = 0x0000 2047d = 0x07FF Storage Form is in Little Endian.
TYPE4	Interrupt threshold	unsigned 2 byte. 0d = 0x0000 2047d = 0x07FF Storage Form is in Little Endian.

16-2. Register Map

The table below provides a listing of the registers. Each address data with is of 8 bit.

Reg.Name	Address	Type	R/W	Set Contents	Remark
Not used	0x00-0x0B	-	-	-	-
STB	0x0C	TYPE1	-	Self-test response	-
INFO	0x0D/0x0E	×	R	More Info	-
WIA	0x0F	TYPE1	R	Who I am	-
DATAX	0x10/0x11	TYPE3	R	X Output value	-
DATAY	0x12/0x13	TYPE3	R	Y Output value	-
DATAZ	0x14/0x15	TYPE3	R	Z Output value	-
INS1	0x16	TYPE1	R	Interrupt source1	-
Not used	0x17	-	-	-	-
STAT1	0x18	TYPE1	R	Status1	-
Not used	0x19	-	-		-
INL	0x1A	TYPE1	R	Interrupt release	-
CNTL1	0x1B	TYPE1	R/W	Control setting 1	-
CNTL2	0x1C	TYPE1	R/W	Control setting 2	-
CNTL3	0x1D	TYPE1	R/W	Control setting 3	-
INC1	0x1E	TYPE1	R/W	Interrupt Control1	-
Not used	0x1F	-	-	-	-
ITHR1	0x26/0x27	TYPE4	R/W	Interrupt threshold	-
-	0x28-0x2F	-	-	Reserved	-
PRET	0x30	TYPE1	R/W	Preset time	-
-	0x46-0x5F	-	-	Reserved	-
TEMP	0x60/0x61	TYPE4	R	Temperature value	-
OFFX	0x6C/0x6D	TYPE4	R/W	Offset X value	-
OFFY	0x72/0x73	TYPE4	R/W	Offset Y value	-
OFFZ	0x78/0x79	TYPE4	R/W	Offset Z value	-
-	0x7A-0xE7	-	-	Reserved	
VER	0xE8/0xE9	TYPE4	R	Firmware version	-
SN	0xEA/0xEB	TYPE4	R	Serial Number	-
-	0xEC-0xFF	-	-	Reserved	

Note1) Please communicate TYPE3 and TYPE4 bringing 2bytes together.

16-3. Register Map Details

"Self-Test Response " Register

Self-Test Response

Register	Type	Main Usage
STB	8bit / R	Self test response

	address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
STB	0x0C	STB=0x55 set of STC/CRTL3=1-> STB=0xAA After reading STB ->STC/CRTL3=0 and STB=0x55							

"Information " Register

Information

Register	Type	Main Usage
INFO	16bit / R	-

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
INFO	0x0D	X	X	X	X	X	X	X	X
	0x0E	X	X	X	X	X	X	X	X

"Who I Am " Register

Who I Am

Register	Type	Main Usage
WIA	8bit / R	Identify byte

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
WIA	0x0F	0x47							

" Output value " Registers

X Output value

Register	Type	Main Usage
DATAX	16bit / R	X channel measurement result

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
DATAX	0x10	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0x11	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

Y Output value

Register	Type	Main Usage
DATAY	16bit / R	Y channel measurement result

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
DATAY	0x12	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0x13	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

Z Output value

Register	Type	Main Usage
DATAZ	16bit / R	Z channel measurement result

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
DATAZ	0x14	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0x15	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

"Interrupt source " Register

Interrupt source

Register	Type	Main Usage
INS1	8bit / R	To hold the Interrupt event with each axis measure.

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
INS1	0x16	PXSI	PYSI	PZSI	NXSI	NYSI	NZSI	NZSI	-

bit	Name	Contents	Default
7	PXSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in positive X-axis. After setting of 1, it is cleared by reading INL.	0
6	PYSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in positive Y-axis. After setting of 1, it is cleared by reading INL	0
5	PZSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in positive Z-axis. After setting of 1, it is cleared by reading INL	0
4	NXSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in negative X-axis. After setting of 1, it is cleared by reading INL.	0
3	NYSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in negative Y-axis. After setting of 1, it is cleared by reading INL	0
2	NZSI	1= When Interrupt event (Beyond the threshold of ITHR1) occurrs in negative Z-axis. After setting of 1, it is cleared by reading INL	0
1	MROI	Out of measurement range (range overflow) (in common throughout all axes)	0
0	-	-	-

"Status" Register

Status1

Register	Type	Main Usage
STA1	8bit / R	Store pin output information

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
STA1	0x18	RES	DRDY	DOR	INT	-	-	-	-

bit	Name	Contents	Default
7	RES	Reserved	-
6	DRDY	This bit is output to the DRDY to inform the preparation status of the measuring data 0: Not ready NG 1: Ready OK	0
5	DOR	Set 1 = In case the measurement results have not been read out during inactivity time ・After setting of 1, it is cleared by reading command.	0
4	INT	This bit is output to the INT to inform the Interrupt event. 0 = No Interrupt event 1 = Interrupt event occurred ・ INS1 tells in which axis the event occurred. ・After setting of 1, it is cleared by reading INL.	0
3	-	-	-
2	-	-	-
1	-	-	-
0	-	-	-

"Interrupt release" Register

Interrupt release

Register	Type	Main Usage
INL	8bit R	By reading the actual register INS1 and STA:INT bit is cleared.

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
INL	0x1A	-	-	-	-	-	-	-	-

"Control Setting" Register

Control Setting1

Register	Type	Main Usage
CNTL1	8bit R/W	Set the Power mode and Measure mode

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
CNTL1	0x1B	PC1	PC2	SC	ODR1	ODR2-	ODR3	FS1	FS2

bit	Name	Contents	Default
7	PC1	Set Power Mode1 0 = stand-by 1 = active	0
6	PC2	Reserved	0
5	SC	Reserved	0
4	ODR1	Set Out Data rate1 0 = 10 SPS(10Hz) 1 = 20 SPS (20Hz)	0
3	ODR2	Reserved	0
2	ODR3	Reserved	0
1	FS1	Set Measurement Mode. 0 = Normal 1 = Force	1
0	FS2	Reserved	0

Control Setting2

Register	Type	Main Usage
CNTL2	8bit / R/W	Set to the Enable or Disable for Interrupt or DREN pin

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
CNTL2	0x1C	RES	RES	RES	IEN	DREN	DRP	RES	RES

bit	Name	Contents	Default
7	RES	Reserved	0
6	RES	Reserved	0
5	RES	Reserved	0
4	IEN	Set the enable for INT 0 = Disable 1 = Enable	0
3	DREN	Set the enable for DRDY 0 = Disnable 1 = Enable	0
2	DRP	Set the Acive for DRDY 0 = low 1 = high	1
1	RES	Reserved	0
0	RES	Reserved	0

Control Setting3

Register	Type	Main Usage
CNTL3	8bit / R/W	Set the control parameter

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
CNTL3	0x1D	SRST	FORCE	RES	STC	-	-	-	-

bit	Name	Contents	Default
7	SRST	Soft reset, perform to same routine as POR 0 = no action 1 = start immediately POR routine -This bit is reset to zero after POR routine	0
6	FORCE	Starts forced measurement period. 0 = no action 1 = start immediately measurement period -This bit is reset to zero after measurement period Done - Possible only when force mode selected (CNTL1, bit FS1=1)	0
5	RES	Reserved	0
4	STC	Self-test function challenge set 0=no action 1=sets 0xAA to STB register, when STB register read, set this bit = 0 and also STB =0x55	0
3	RES	Reserved	0
2	RES	Reserved	0
1	RES	Reserved	0
0	RES	Reserved	0

"Interrupt control" Register

Interrupt control 1

Register	Type	Main Usage
INC1	8bit / R/W	Set of Interrupt Control Parameter.

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
INC1	0x1E	XIEN	YIEN	ZEN	-	IEA	IEL	-	-

bit	Name	Contents	Default
7	XIEN	Enable X-axis Interrupt 0 = Disable 1 = Enable	1
6	YIEN	Enable Y-axis Interrupt 0 = Disable 1 = Enable	1
5	ZEN	Enable Z-axis Interrupt 0 = Disable 1 = Enable	1
4	-	-	0
3	IEA	Set Interrupt Active 0 = low 1 = high	1
2	IEL	Set Interrupt Signal 0 = latched 1 = one pluse(0.05ms)	0
1	--	-	0
0	--	-	-

" Interrupt threshold" register

Set the Interrupt threshold. . Data size is 2 byte. The set values are as given below:
Use the In Interrupt threshold for three-axis

Interrupt threshold1

Register	Type	Main Usage
ITHR1	16bit / R/W	Set Interrupt threshold

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
ITHR1	0x26	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0x27	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

"Preset Time" register

Preset Time

Register	Type	Main Usage
PRET	8bit / R/W	Preset time before measurement

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
PRET	0x30	-	-	-	-	PS3	PS2	PS1	PS0

bit	Name	Content	Default
7	-	-	0
6	-	-	0
5	-	-	0
4	-	-	0
3	PS3	-	0
2	PS2	-	0
1	PS1	-	0
0	PS0	--	0

"Temperature sensor output value" Register

Temperature sensor output value

Register	Type	Main Usage
TEMP	16bit / R	Temperature code

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
TEMP	0x60	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0x61	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

"Offset" registers

Set the electronic movement point. Data size is 2 bytes. The default value in different for each pieces. The set values are as given below:

Offset X

Register	Type	Main Usage
OFFX	16bit / R/W	X-axis offset adjusting

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
OFFX	0x6C	Reserved	X	X	X	X	X	X	X
	0x6D	Reserved							

Offset Y

Register	Type	Main Usage
OFFY	16bit / R/W	Y-axis offset adjusting

	Address	7bit	6bit	5b	4bit	3bit	2bit	1bit	0bit
OFFY	0x72	Reserved	X	X	X	X	X	X	X
	0x73	Reserved							

Offset Z

Register	Type	Main Usage
OFFZ	16bit / R/W	Z-axis offset adjusting

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
OFFZ	0x78	Reserved	X	X	X	X	X	X	X
	0x79	Reserved							

" Firmware version" Register

Register	Type	Main Usage
VER	16bit / R	Firmware version

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
VER	0xE8	RES	Firmware version						
	0xE9	RES	RES	RES	RES	RES	RES	RES	RES

" Serial Number" Register

Register	Type	Main Usage
SN	16bit / R	Serial Number

	Address	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
SN	0xEA	LSB7	LSB6	LSB5	LSB4	LSB3	LSB2	LSB1	LSB0
	0xEB	MSB7	MSB6	MSB5	MSB4	MSB3	MSB2	MSB1	MSB0

[17] Reliability Test Conditions

No.	Test Item	Test Condition [In accordance to EIAJ ED-4701]	＊1. Preparation	Test-Time	n(C=0) [LTPD]	Criterion
1	High Temp. Storage	Ta= +125°C	No	500 hours	22 [10%]	Change rate of the electro-magnetic characteristics must be less than ±20% .
2	Low Temp. Storage	Ta= -40°C	No	500 hours	22 [10%]	
3	Temperature Humidity Storage	Ta= +85°C, RH= 85%	1) + 2)	500 hours	22 [10%]	
4	High Temp. Bias	Ta= +125°C, VDD= +3.6V	No	500 hours	22 [10%]	
5	High Temp. Humidity Bias	Ta= +85°C, RH= 85%, VDD= +3.6V	1) + 2)	500 hours	22 [10%]	
6	Temperature Cycle Test	-40°C ↔ +125°C (30min－5min－30min)	1) + 2)	10 cycles	22 [10%]	
7	Thermal shock	-40°C ↔ +125°C (5min－10s－5min)	1) + 2)	10 cycles	22 [10%]	
8	Solder Heat Resistance	Infrared Reflow（See graph below: High temp. Reflow peak is below 260°C）	1)	3 times	22 [10%]	
9	ESD Sensitivity	C= 100pF, R= 1.5k ohm, ±2kV (Min.)	No	3 times	22 [10%]	
10	CDM Sensitivity	±500V	No	1 time	22 [10%]	
11	Circuit Board Flex	Support Span 90mm, Flex 3mm、5±1second hold	No	1 time	22 [10%]	
12	Solderability	Ta= +235°C	3)	3 seconds	22 [10%]	Covered with solder more than 95% of the dipped portion of the terminal.
13	Sensor Body Strength	R0.5 pressure jig, 10N、10±1sec hold	No	1 time	22 [10%]	Mechanical Characteristics

［ Preparation conditions］（Ref.: EIAJ ED4701-2 B101A）

1) Saturation Humidification processing :
   (Ta= +85°C, RH= 30%, t= 168 hours, + Ta= +30°C, RH= 70%, t= 168 hours)
2) Infrared Reflow (continuously for 3 times)
3) Water vapor aging (4 hours）

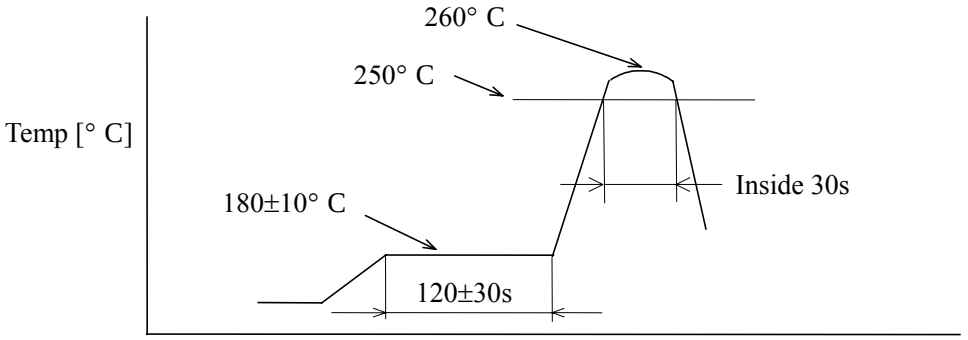
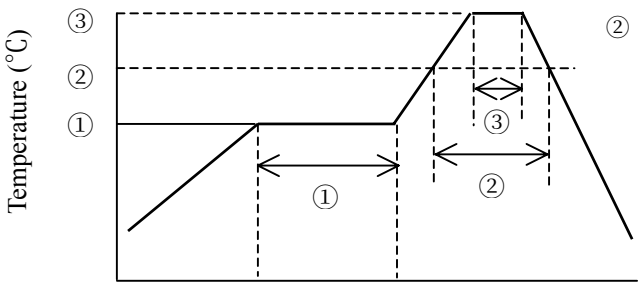


Fig.1. Infrared Reflow Heating Conditions

[18] Solder reflow condition

Solder reflow condition is shown below.



① Preheating：(+150～+190℃) × (90±30sec.)

② +220℃ marginal zone：20～50sec.

③ Heating：+235～+250℃ peak (within 10sec.)

④ Heating environment：air or N_2

⑤ Number of Reflow times：2

Fig.2. Solder reflow condition

Repair should be carried out with following conditions : +250～+270℃×within 30 sec.

Heating time + within 150 sec. (Including preheating time 70sec.)

In case moisture absorbent products are used, the repair should be carried out after baking.

[19] Notes

1) This device uses a C-MOS IC. Please take precautions to prevent damage due to electrical static discharge.
2) In order to obtain stable operation please place a X5R ceramic capacitor (capacity more than 1.0μF) between AVDD-GND a X5R ceramic capacitor (capacity more than 0.01μF) between DVDD-GND. Please set these capacitors in neighborhood to the pins.
3) The writing pattern to AVDD and GND hold be as wide as possible in order to reduce high frequency impedance.
4) Storage Method (moisture-proof and packed condition)
   a) Please do not leave the device in the following environments:
   * High temperature and high humidity
   * Places with direct sun light
   * Places with extreme temperature changes
   * Dusty places
   * In corrosive gas
   b) Recommended storage temperature and humidity:
   * +5℃～+30℃, below 70%RH, please use device within one year.
   (If the device does not use over one year, the specification may not be satisfied.)
5) Usage after opening the moisture-proof package
   a) Please apply devices within 7days under the condition of +5℃～+30℃、below 70%RH.
   The storage in the moisture-proof room (+5℃～+30℃、below 30%RH) is recommended.
   b) When the devices storage in the moisture- proof room (+30℃、below10%RH), please apply them within 1 year.
   c) Over 7days after opening the package with a) condition above, please apply baking according to the following conditions.

＜Baking condition＞

i) +60℃×168Hr or +40℃×200Hr by taping condition

ii) +125℃×24Hr by heat resistant tray

iii) Maximum 2 times for baking

※ It is recommended to wear out after opening package for the first time.

6) Please short-circuit the 2 GND pins with thick and short wiring.

7) OTP memory in this product is not rewritable.

8) To assure stable functioning, set a ceramic capacitor of not less than 1.0uF between AVDD-GND terminals, and a ceramic capacitor of not less than 0.01uF between DVDD-GND terminals.

9) Sensor property may change due to the heat effect during PCB mounting. We recommend to calibrate the sentitivity and origin point of magneitc sensors after mounting

10) Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near the ferromagnetic parts.